

SN74LS156N**■ Product Introduction**

The SN74LS156N circuit features dual 2-line-to-4-line demultiplexer with individual strobes and common binary-address input. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired.

■ Product Features

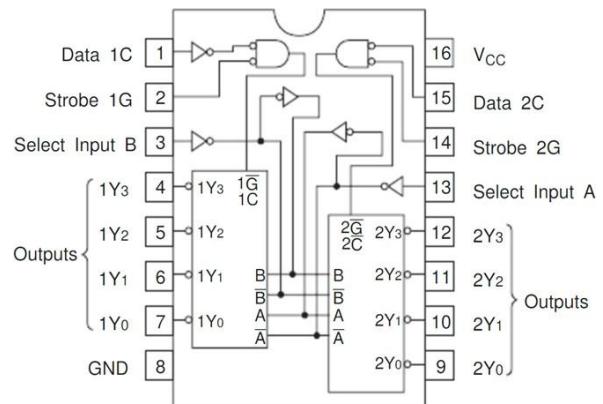
- Permits use as a 3-to-8-line decoder or 1-to-8-line or 1-to-4-line demultiplexer
- Fully compatible with TTL/DTL input logic level
- The common binary-address inputs sequentially select of 2-to-4-line decoder
- Open drain output structure
- Package format: DIP16, SOP16

■ Product Applications

- Digital logic driver
- Industrial control application
- Other application areas

■ Package and Pin Assignment

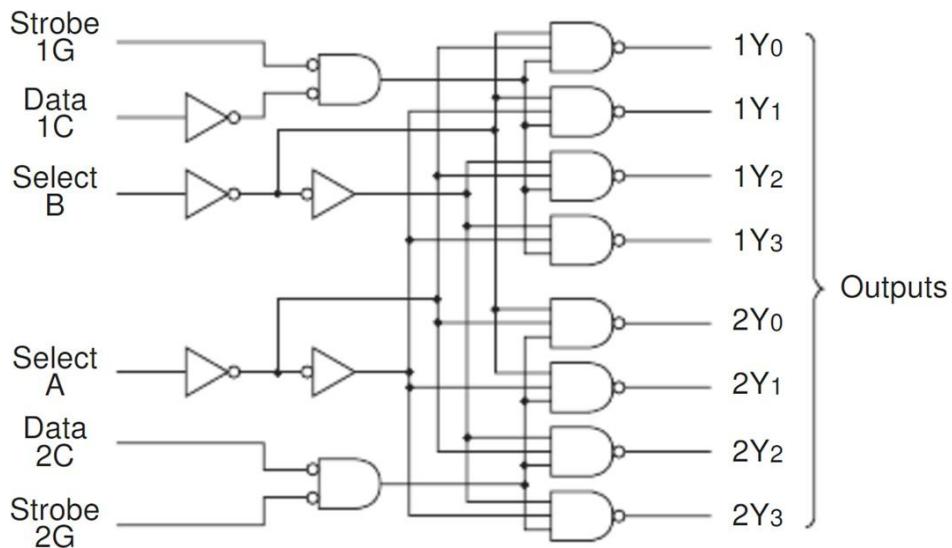
SOP16 or DIP16			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Data 1C	16	Supply VCC
2	Strobe 1G	15	Data 2C
3	Select Input B	14	Strobe 2G
4	Output 1Y3	13	Select Input A
5	Output 1Y2	12	Output 2Y3
6	Output 1Y1	11	Output 2Y2
7	Output 1Y0	10	Output 2Y1
8	Supply GND	9	Output 2Y0

**■ Absolute Maximum Ratings**

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V _{cc}	7	V
Input voltage	V _I	7	V
Power dissipation	P _D	500	mW
Operating temperature	T _A	0-70	°C
Storage temperature	T _S	-65-150	°C
Welding temperature	T _w	260,10s	°C

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

■ Block Diagram



■ Function Table

2-line-to-4-line Decoder

1-line-to-4-line Demultiplexer

Inputs			Outputs			
Select	Strobe	Data	1Y0	1Y1	1Y2	1Y3
B	A	G1	C1			
X	X	H	X	H	H	H
L	L	L	H	L	H	H
L	H	L	H	H	L	H
H	L	L	H	H	H	L
H	H	L	H	H	H	L
X	X	X	L	H	H	H

2-line-to-4-line Decoder

1-line-to-4-line Demultiplexer

Inputs			Outputs			
Select	Strobe	Data	2Y0	2Y1	2Y2	2Y3
B	A	G2	C2			
X	X	H	X	H	H	H
L	L	L	L	H	H	H
L	H	L	L	H	H	H
H	L	L	L	H	L	H
H	H	L	L	H	H	L
X	X	X	H	H	H	H

3-line-to-8-line Decoder / 1-line-to-8-line Demultiplexer

Inputs			Outputs							
Select	Strobe Or Data	G	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C	B	A	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H
H	H	L	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	L

C = inputs C1 and C2 connected together

G = inputs G1 and G2 connected together

H = high level, L = low level, X = don't care

■ Recommended Operating Conditions

Item	Symbol	Min	Tpy	Max	Unit
Supply voltage	V _{CC}	4.75	5.00	5.25	V
Output voltage	V _{OFF}	—	—	5.5	V
Output current	I _{OL}	—	—	8	mA
Operating temperature	T _{opr}	0	25	60	°C

■ Electrical Characteristics(T_A=25°C, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions
Input voltage	V _{IH}	2	—	—	V	VCC=4.75V, V _{IH} =2 VV _{IL} =0.7V
	V _{IL}	—	—	0.7	V	
Output current	I _{OH}		0.1	100	uA	V _{OH} =-5.5V
Output voltage	V _{OL}	—	0.12	0.4	V	I _{OL} =4mA
		—	0.22	0.5		I _{OL} =8mA
Input current	I _{IH}	—	0.1	20	uA	VCC=5.25V, V _I =2.7V
	I _{IL}	—	0.23	-0.4	mA	VCC=5.25V, V _I =0.4V
	I _I	—	0.1	100	uA	VCC=5.25V, V _I =7V
Supply current *	I _{CC}	—	6	10	mA	VCC=5.25V
Input clamp voltage	V _{IK}	—	0.9	-1.5	V	VCC=4.75V, I _I =-18mA

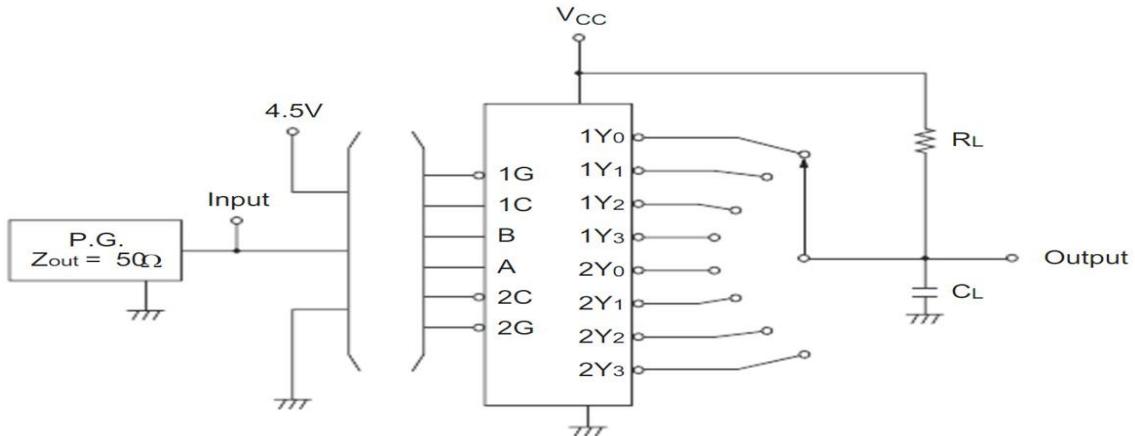
Notes: * ICC is measured with all outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 grounded.

■ Switching Characteristics(T_A=25°C, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions
Propagation delay time A、B、2C、1G or 2G	t _{PLH}	—	20	—	ns	V _{CC} =5V C _L =16pF R _L =2K
	t _{PHL}	—	25	—	ns	
Propagation delay time A or B to Outputs	t _{PLH}	—	20	—	ns	V _{CC} =5V C _L =16pF R _L =2K
	t _{PHL}	—	25	—	ns	
Propagation delay time 1C to Outputs	t _{PLH}	—	20	—	ns	V _{CC} =5V C _L =16pF R _L =2K
	t _{PHL}	—	20	—	ns	

■ Testing Method

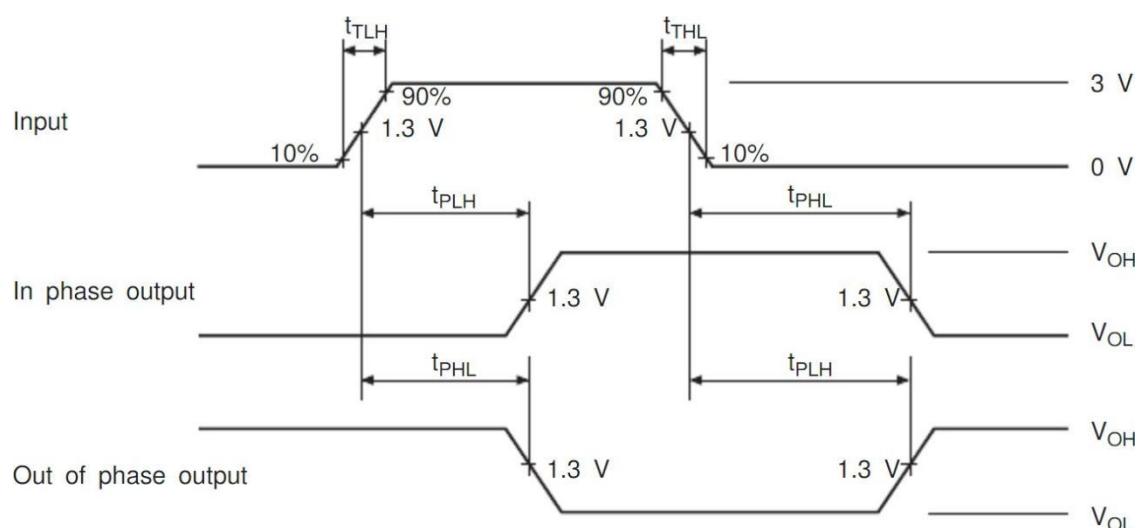
1 ◀ Test Circuit



Notes:

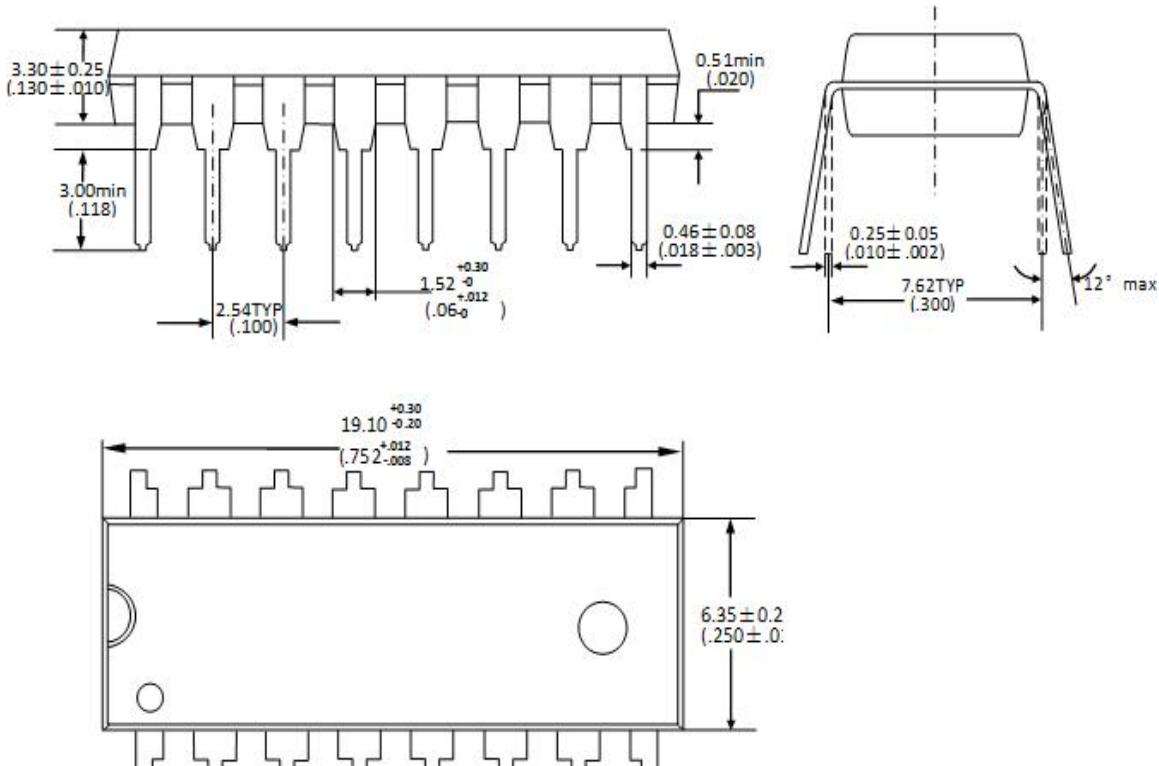
- A. Input signal pulse: $f=1\text{MHz}$, $D=50\%$, $t_{TLH}=t_{THL}$ is less than 20ns, except for special regulations.
- B. The C_L capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.

2 ◀ Waveform



■ Package Dimensions

Unit : mm /inch

DIP16**SOP16**